

FIG 1

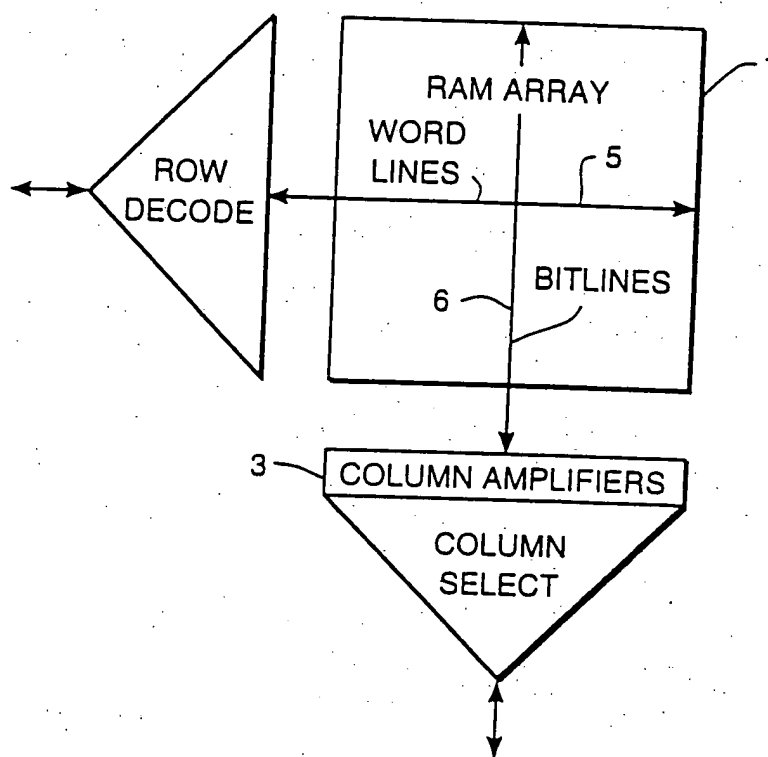


FIG. 2

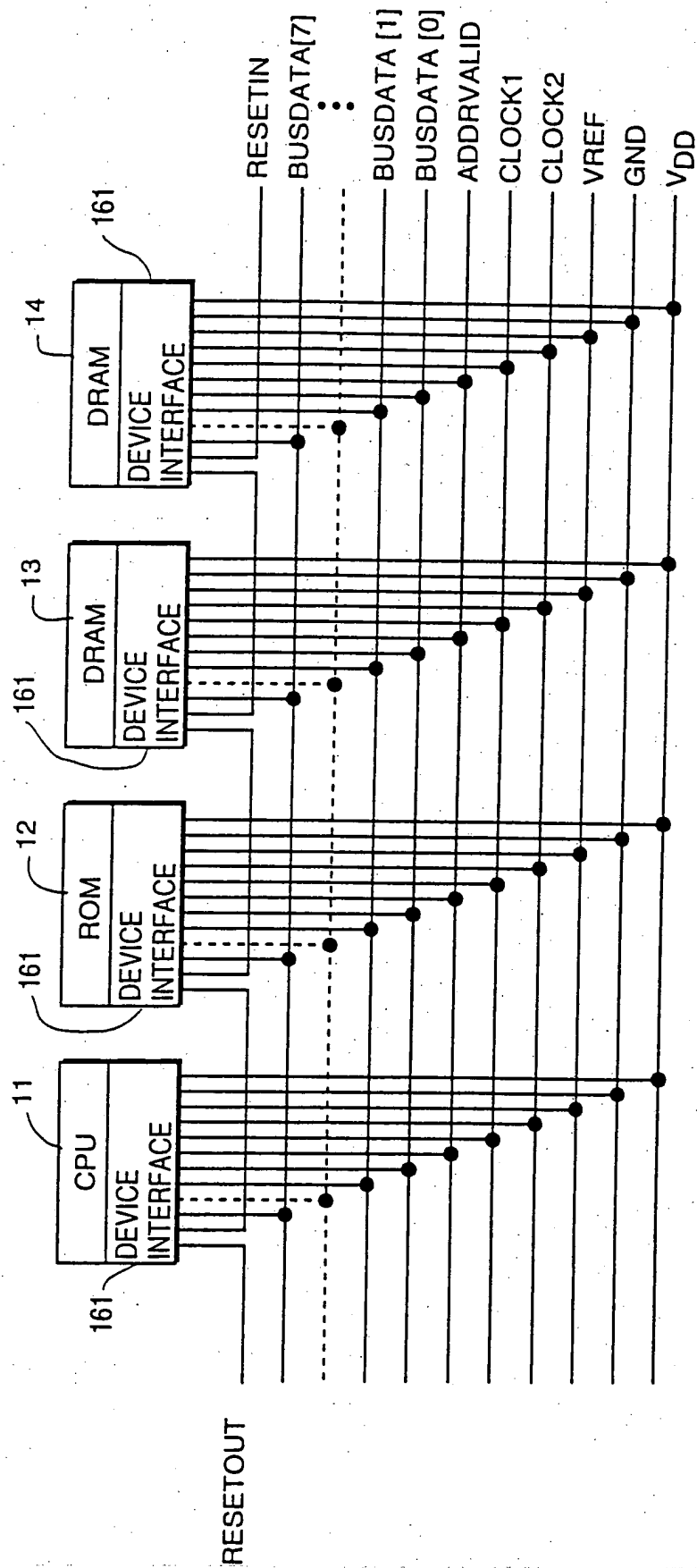
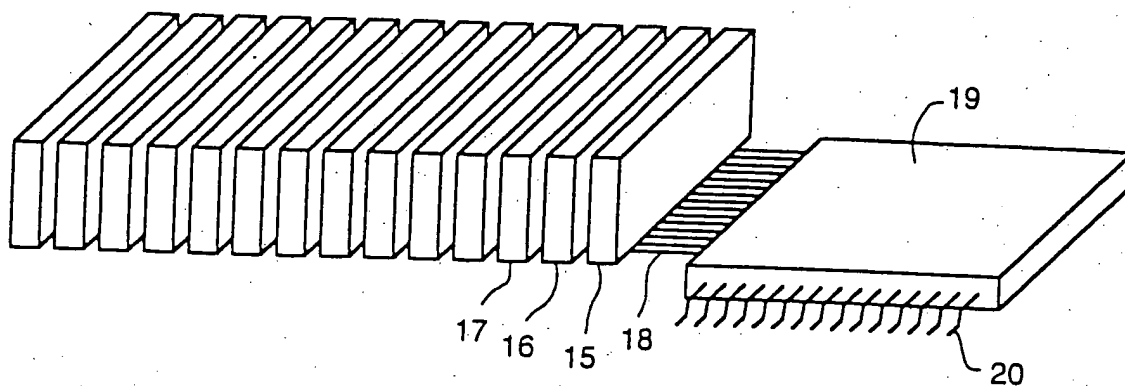


FIG 3



REGULAR ACCESS

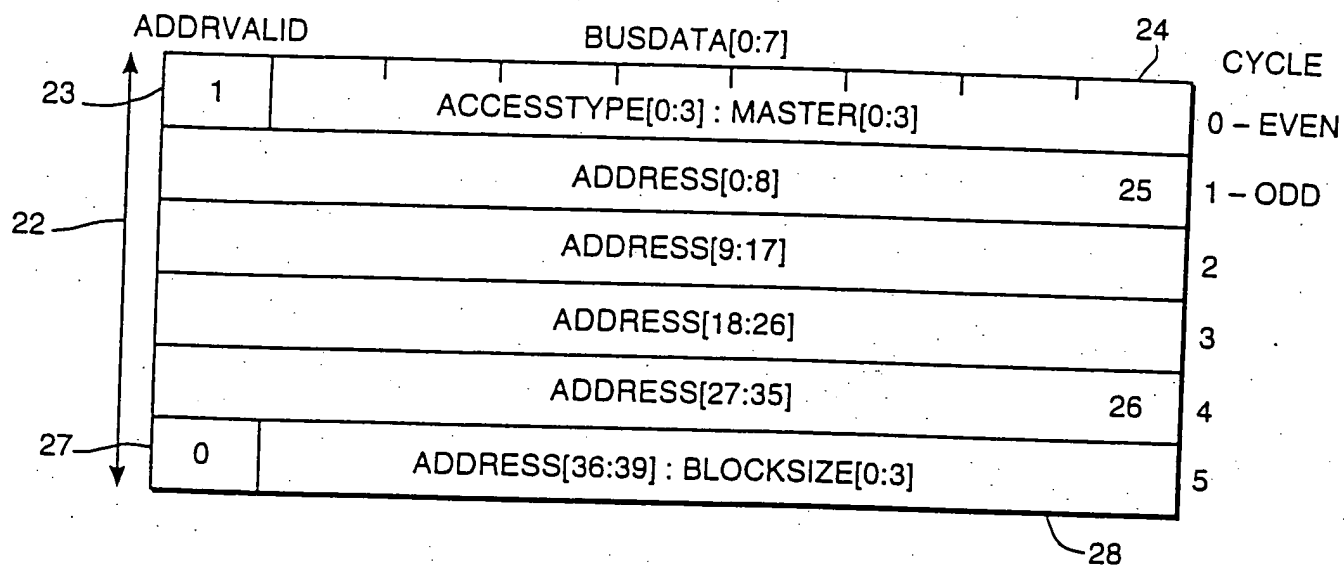


FIG 4

REJECT (NACK) CONTROL PACKET

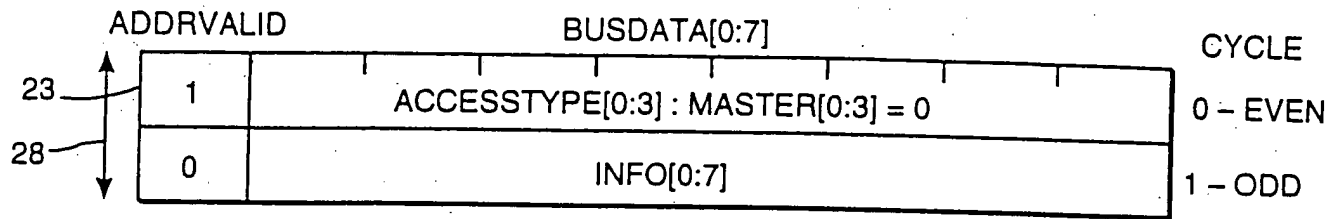


FIG 5

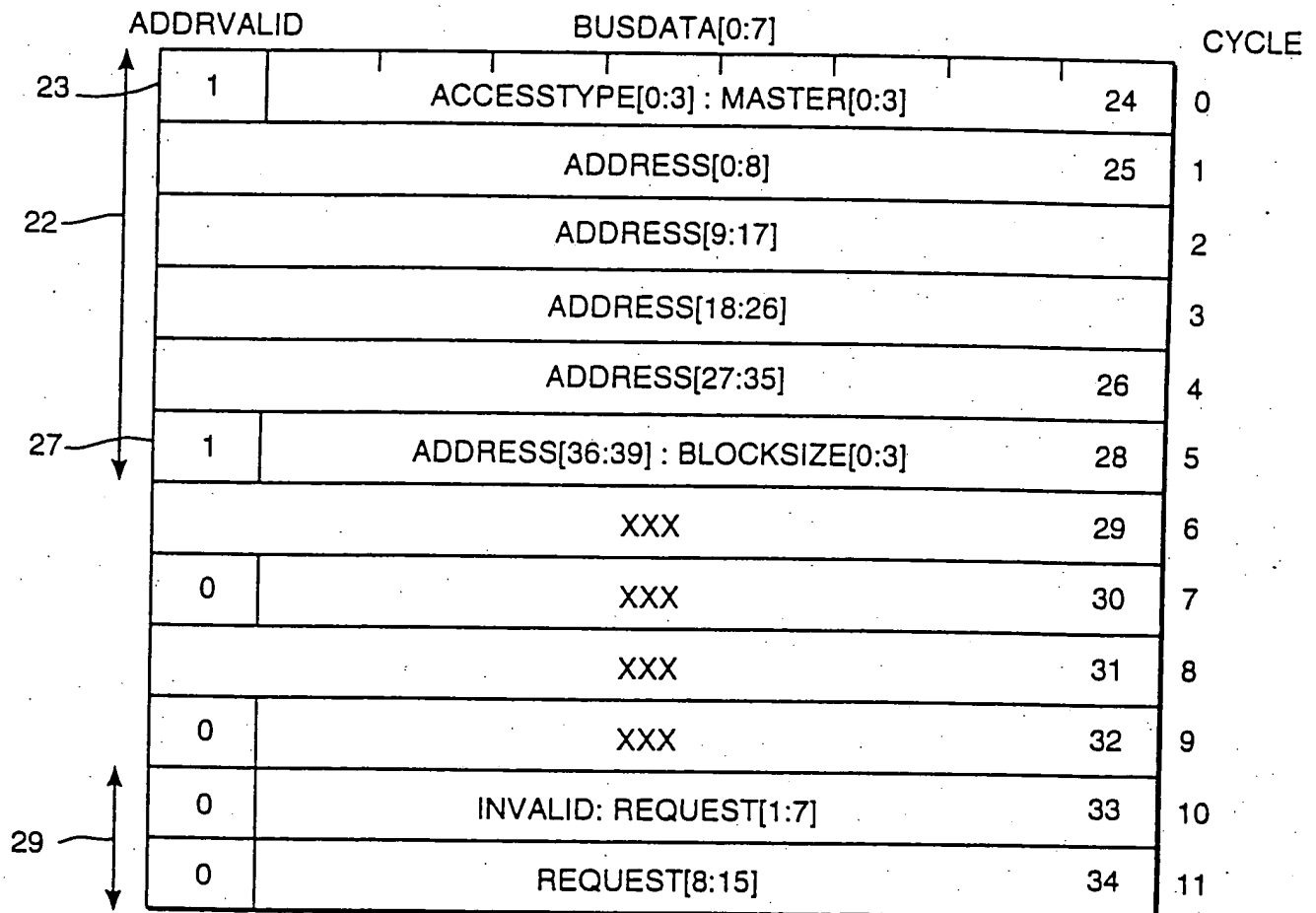


FIG 6

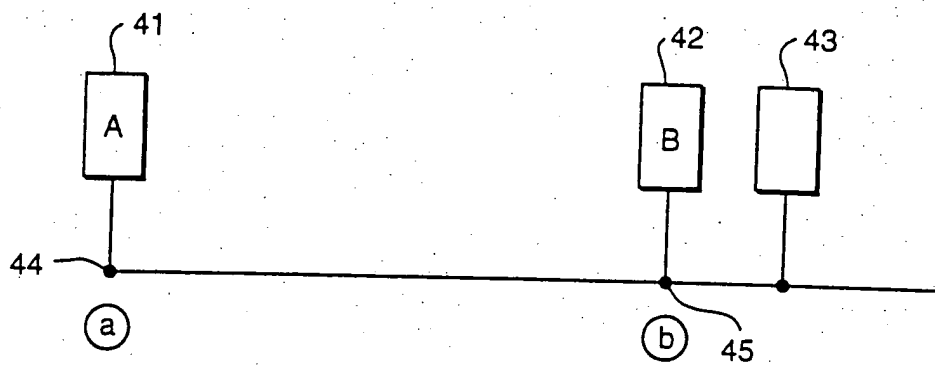
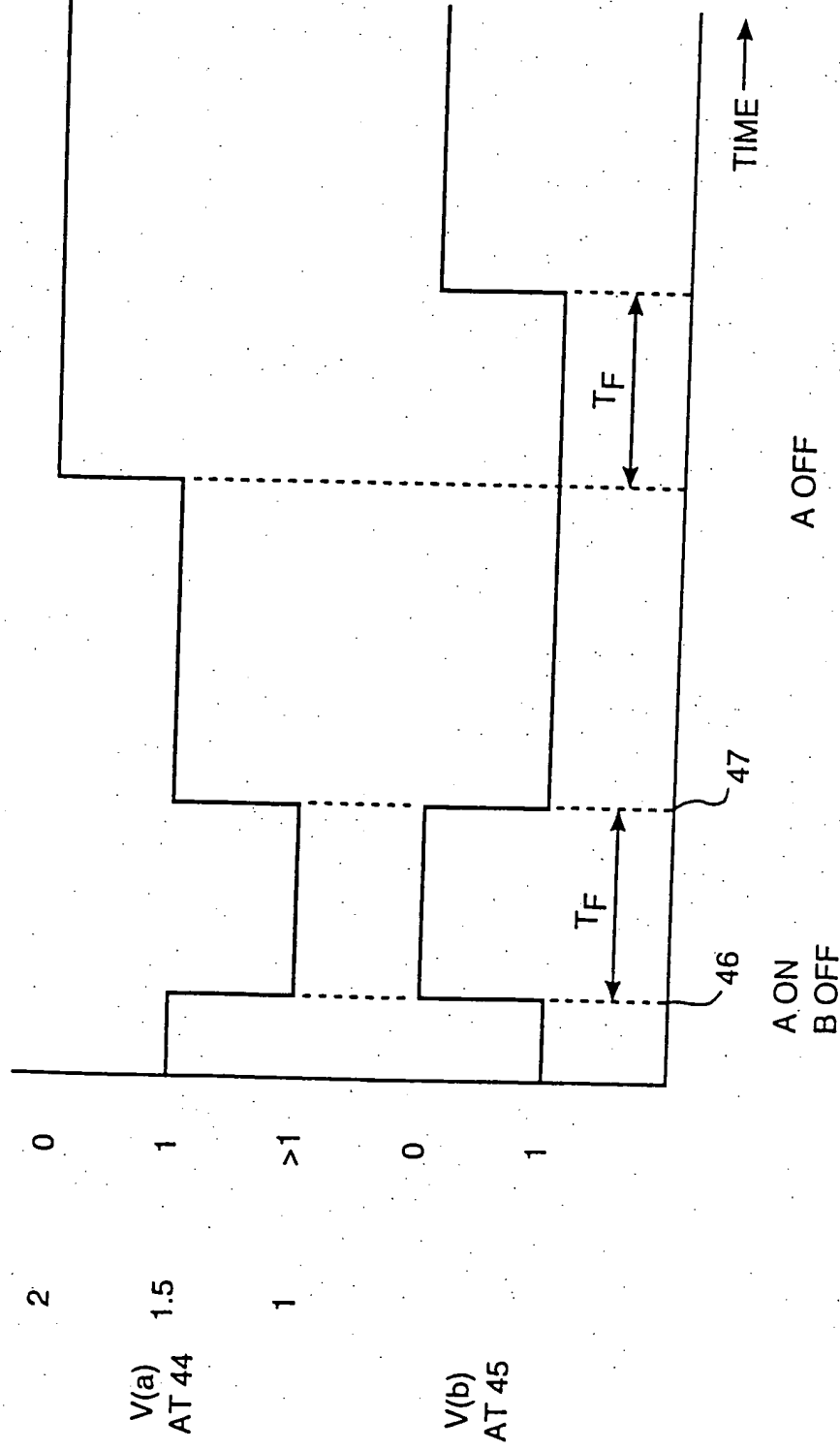


FIG 7A

VOLTAGE LOGICAL
VALUE



FILE 7B

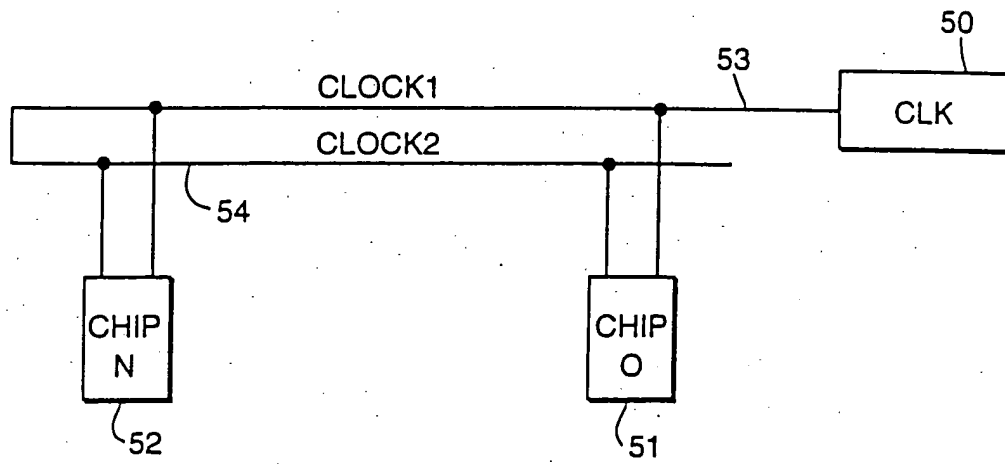


FIG 8A

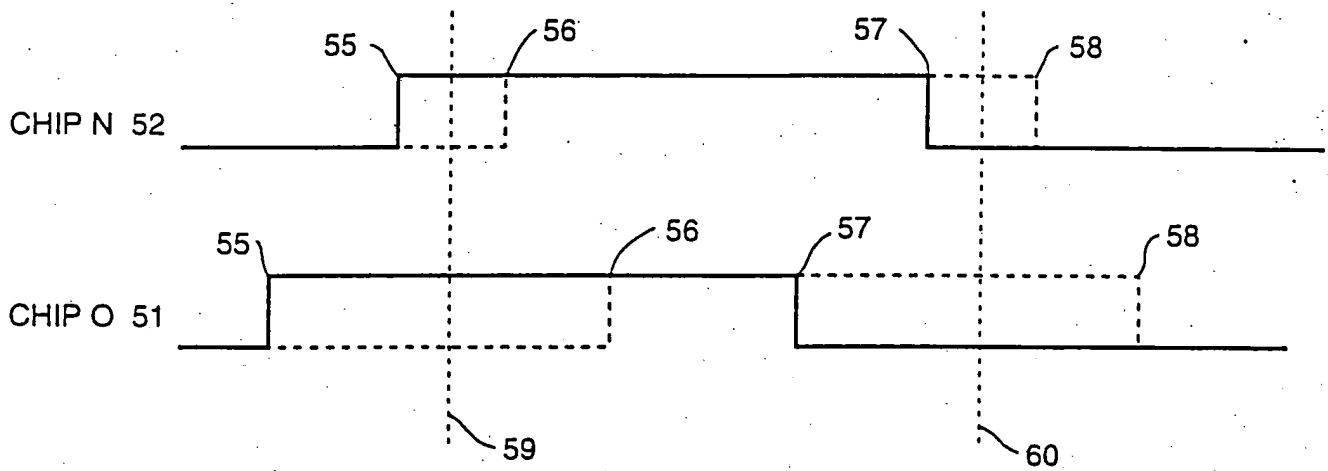
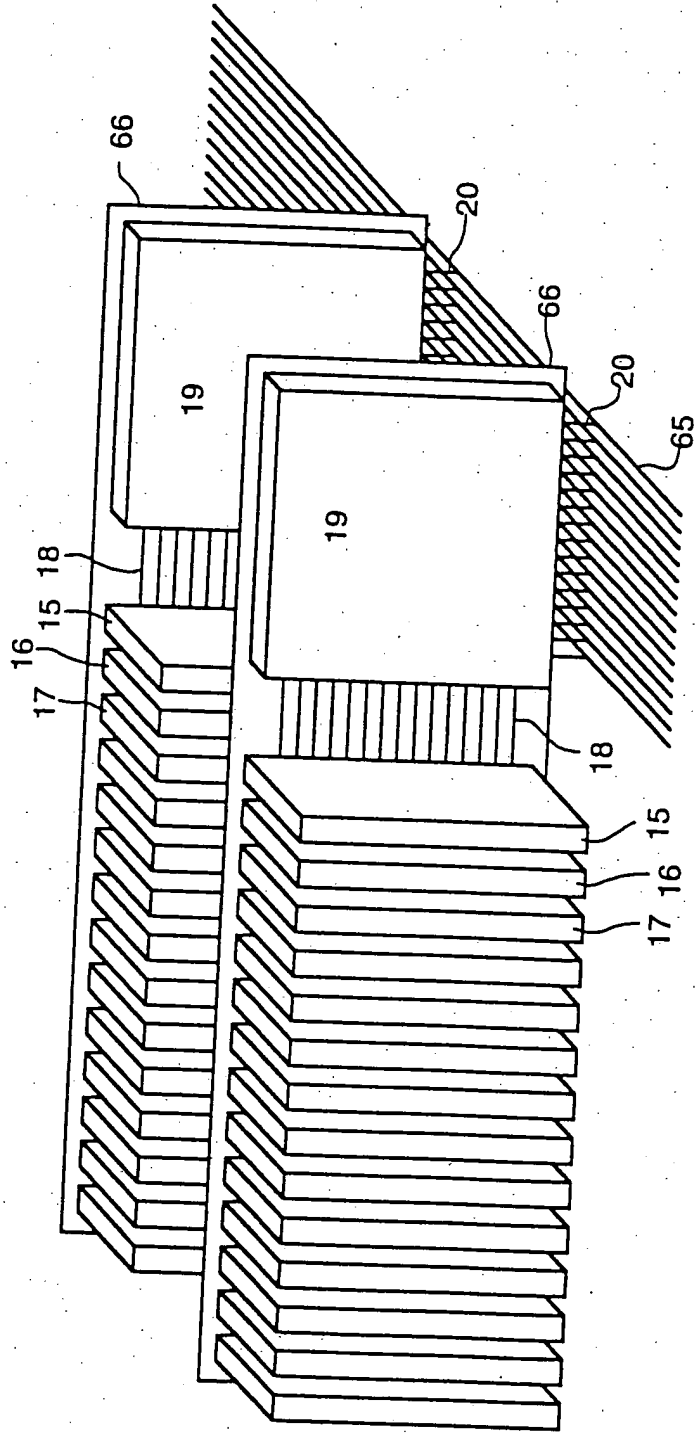


FIG 8B

FIG. 9



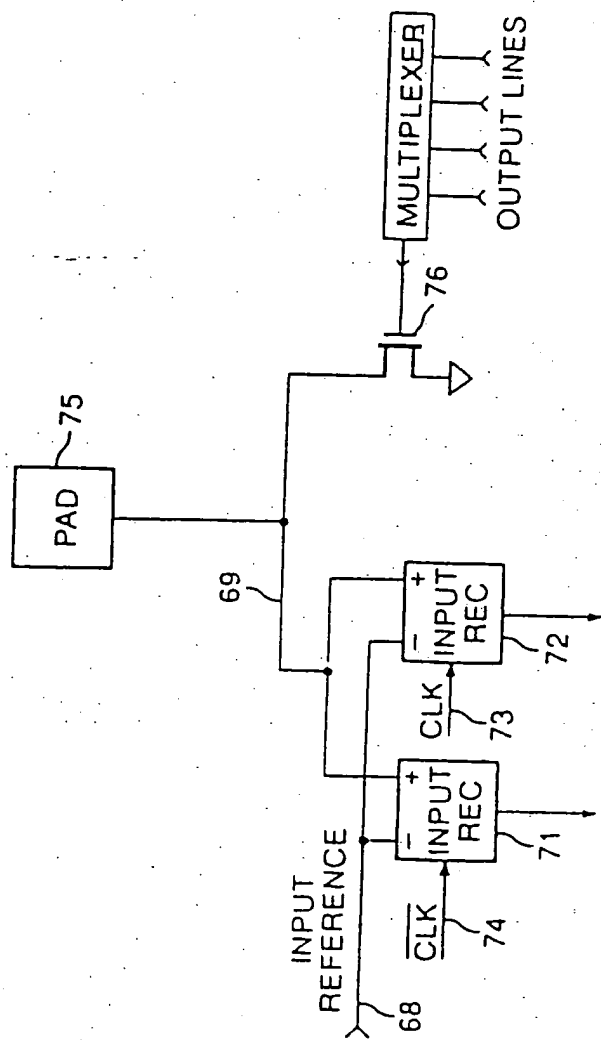


FIG. 10

FIG. 11

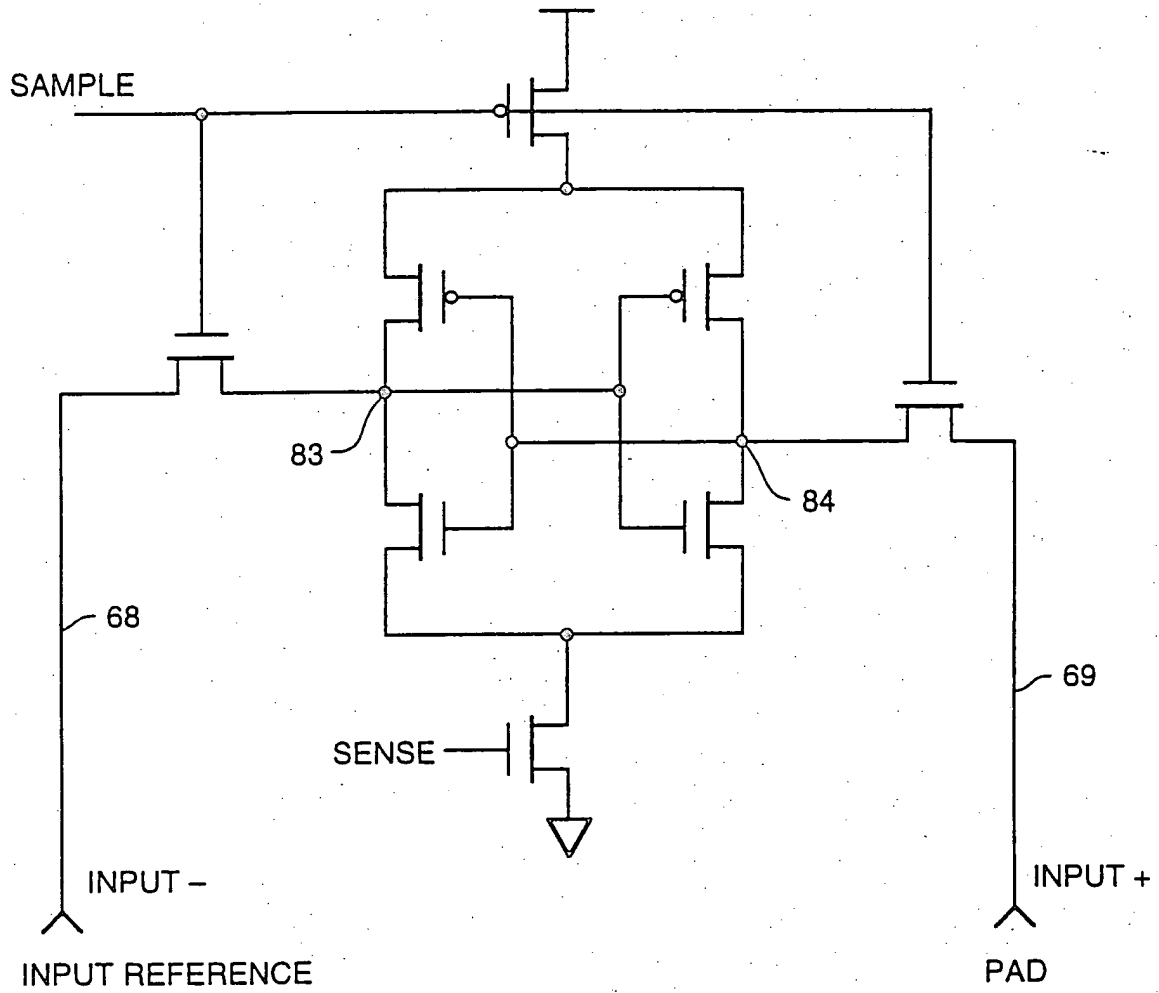


FIG. 12

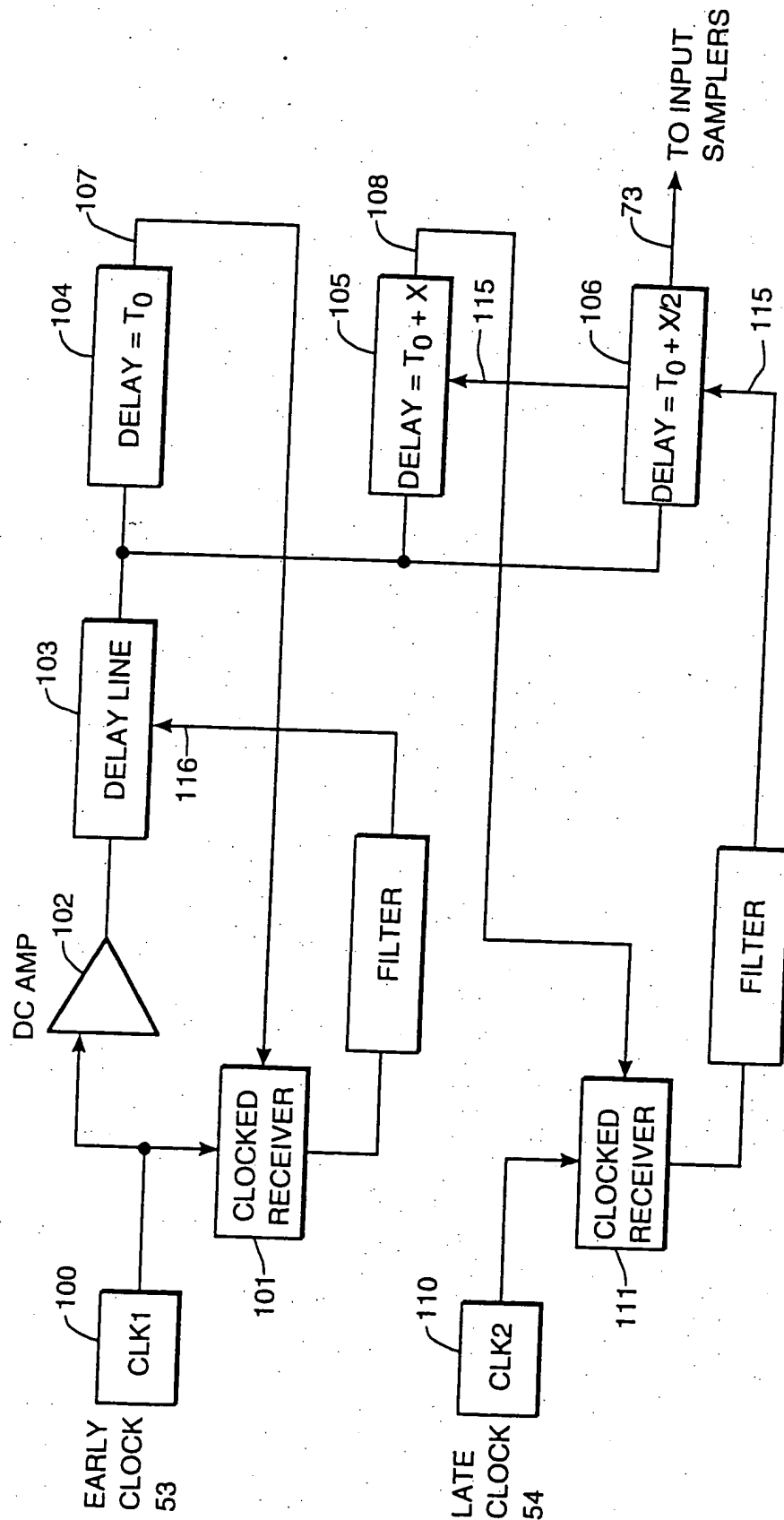
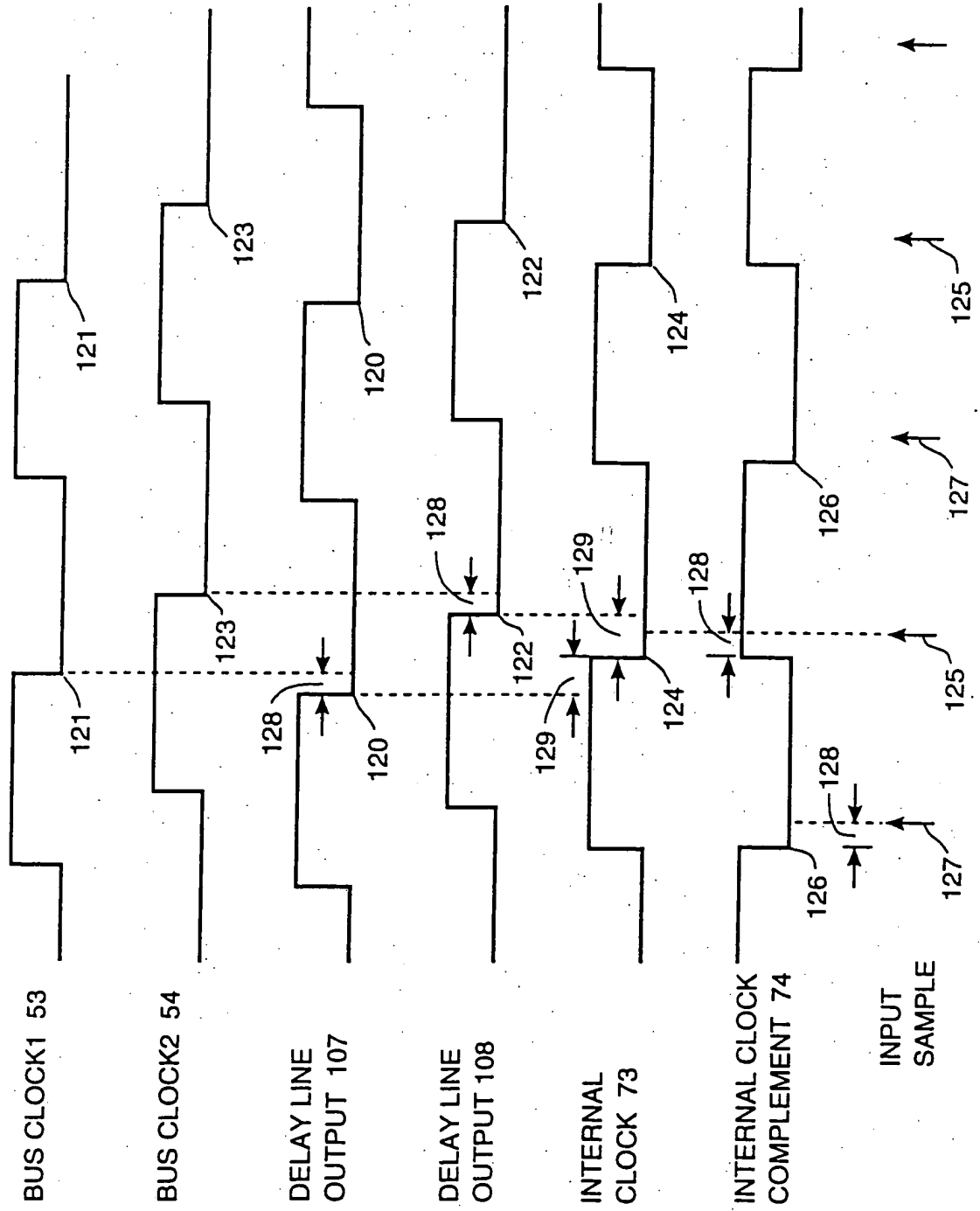


FIG 13



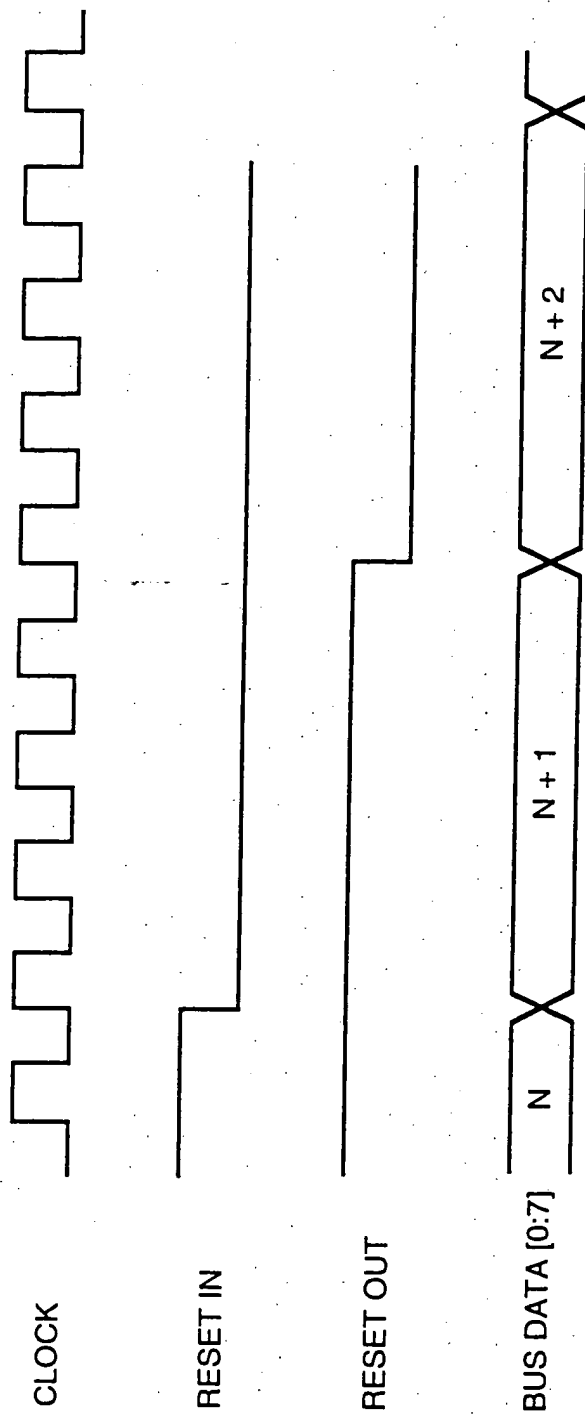


FIG 14

FIG 15

